What is claimed is:

1. A resonant circuit structure comprising:

a load;

a primary component coupled to a node;

a secondary component array coupled to the node, in parallel to the primary component; and

a reduction system, intercoupled between the load and the node, and adapted to reduce to operational voltage at the node to a target value.

2. The structure of claim 1, wherein the resonant circuit structure comprises an inductive load and a capacitance coupled in series.

3. The structure of claim 1, wherein the load comprises an antenna.

4. The structure of claim 1, wherein the primary component comprises a capacitive element.

5. The structure of claim 4, wherein the capacitive element is a capacitor.

6. The structure of claim 4, wherein the secondary component array comprises a capacitive element.

7. The structure of claim 6, wherein the capacitive element is a capacitor.

8. The structure of claim 6, wherein the secondary component array comprises a switchable element.

9. The structure of claim 8, wherein the switchable element is a transistor.

10. A circuitry segment, implementing an RLC resonant circuit structure utilizing integrated and discrete devices, the circuitry segment comprising:

a driver circuit, instantiated within a first integrated semiconductor device;

a primary resistive element, having a first terminal coupled the driver circuit, and a second terminal coupled to a first terminal of an inductive load;

a reduction system, having a first terminal coupled to a second terminal of the inductive load, and having a second terminal coupled to a node;

a primary capacitive element, having a first terminal coupled to the node; and

a secondary component array coupled to the node, in parallel to the primary capacitive element;

wherein the reduction system is adapted to reduce to operational voltage at the node to a target value.

11. The circuitry segment of claim 10, wherein the RLC resonant circuit structure is a low frequency resonant circuit.

12. The circuitry segment of claim 10, wherein the RLC resonant circuit structure is a radio frequency resonant circuit.

13. The circuitry segment of claim 10, wherein the primary resistive element is a resistor.

14. The circuitry segment of claim 13, wherein the resistor is a discrete component.

15. The circuitry segment of claim 10, wherein the inductive load is an antenna.

16. The circuitry segment of claim 15, wherein the antenna is for a base transceiver in a wireless communication system.

17. The circuitry segment of claim 10, wherein the primary capacitive element comprises a capacitor.

18. The circuitry segment of claim 10, wherein the primary capacitive element comprises a plurality of capacitors.

19. The circuitry segment of claim 17, wherein the capacitor is a discrete component.

20. The circuitry segment of claim 17, wherein the capacitor is integrated within a semiconductor device.

21. The circuitry segment of claim 10, wherein the secondary component array comprises a capacitor.

22. The circuitry segment of claim 10, wherein the secondary component array comprises a switchable element.

23. The circuitry segment of claim 22, wherein the switchable element comprises a transistor.

24. The circuitry segment of claim 21, wherein the capacitor is a discrete component.

25. The circuitry segment of claim 21, wherein the capacitor is integrated within a semiconductor device.

26. The circuitry segment of claim 23, wherein the transistor is integrated within a semiconductor device.

27. The circuitry segment of claim 10, wherein the reduction system comprises a capacitor.

28. The circuitry segment of claim 10, wherein the reduction system comprises a plurality of capacitors.

29. The circuitry segment of claim 27, wherein the capacitor is a discrete component.

30. The circuitry segment of claim 27, wherein the capacitor is integrated within a semiconductor device.

31. A method of producing a tunable resonant circuit, having integrated and discrete devices, the method comprising the steps of:

providing a driver circuit instantiated within a first integrated semiconductor device;

providing a primary resistor, having a first terminal coupled the driver circuit, and a second terminal coupled to a first terminal of an inductive load;

providing a primary capacitor, having a first terminal coupled to a node;

providing a secondary capacitor having a first terminal coupled to the node;

providing a transistor having a first terminal coupled to a second terminal of the

secondary capacitor, and a second terminal coupled to ground; and

providing a reduction system, having one or more intercoupled capacitors, a first terminal of which is coupled to a second terminal of the inductive load, and a second terminal of which coupled to the node, adapted to reduce to operational voltage at the node to a target value.

32. The method of claim 31, wherein the step of providing a transistor further comprises providing a transistor instantiated within an integrated semiconductor device.

33. The method of claim 32, wherein the step of providing a transistor further comprises providing a transistor instantiated within the first integrated semiconductor device.

34. The method of claim 31, wherein the step of providing a secondary capacitor further comprises providing a secondary capacitor instantiated within an integrated semiconductor device.

35. The method of claim 34, wherein the step of providing a secondary capacitor further comprises providing a secondary capacitor instantiated within the first integrated semiconductor device.